

# NB2872A

## Low Power, Reduced EMI Clock Synthesizer

The NB2872A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The NB2872A reduces ElectroMagnetic Interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The NB2872A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding that are traditionally required to pass EMI regulations.

The NB2872A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

The NB2872A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

The NB2872A is targeted towards all portable devices with very low power requirements like MP3 players, Notebooks and digital still cameras.

### Features

- Generates an EMI Optimized Clocking Signal at the Output
- Integrated Loop Filter Components
- Operates with a 3.3 V  $\pm$  0.3 V Supply
- Operating Current less than 6.0 mA
- Low Power CMOS Design
- Input Frequency Range: 15 MHz to 30 MHz
- Generates a 1X Low EMI Spread Spectrum clock of the Input Frequency
- Frequency Deviation  $-1.25\%$
- Available in TSOP-6 Package (TSOT-23-6)
- Pb-Free Package is Available



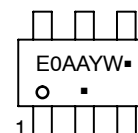
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



TSOP-6  
(TSOT-23-6)  
SN SUFFIX  
CASE 318G



E0A = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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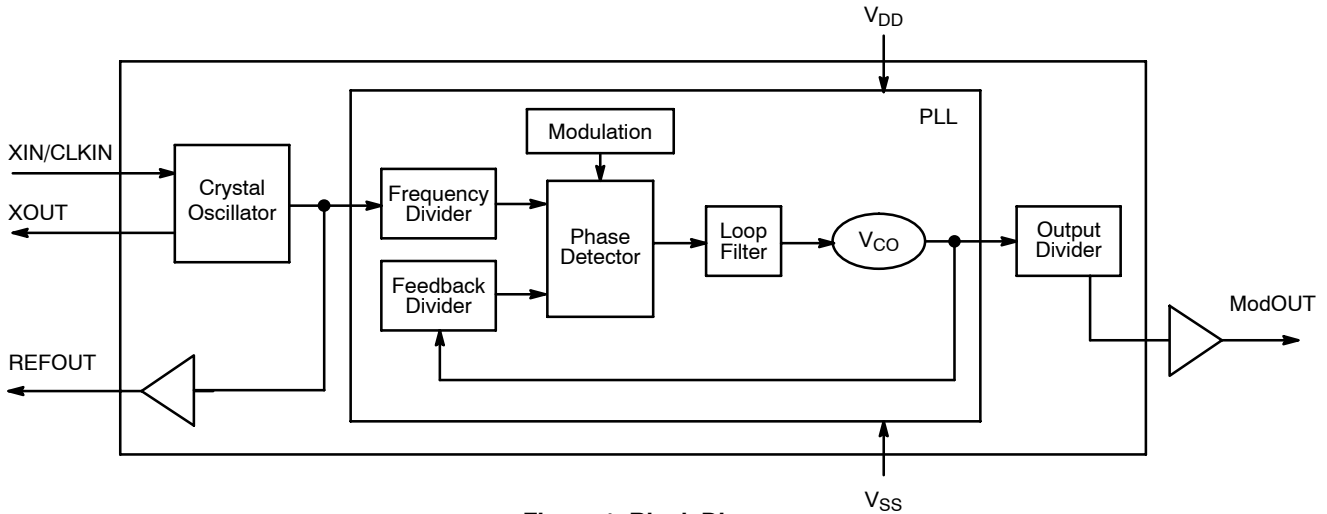


Figure 1. Block Diagram

Table 1. KEY SPECIFICATIONS

Description	Specification
Supply Voltages	$V_{DD} = 3.3\text{ V} \pm 10\%$
Frequency Range	$15\text{ MHz} < \text{CLKIN} < 30\text{ MHz}$
Cycle-to-Cycle Jitter	300 ps (maximum)
Output Duty Cycle	40 / 60% (worst case)
Output Rise and Fall Times	1.1 ns (maximum)
Modulation Equation	$F_{IN}/640$
Frequency Deviation	-1.25%

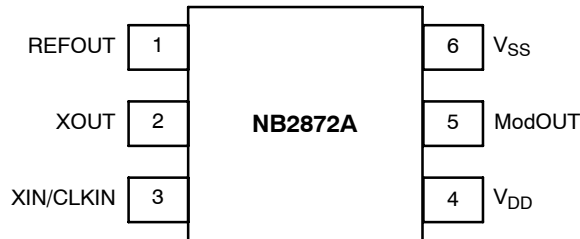
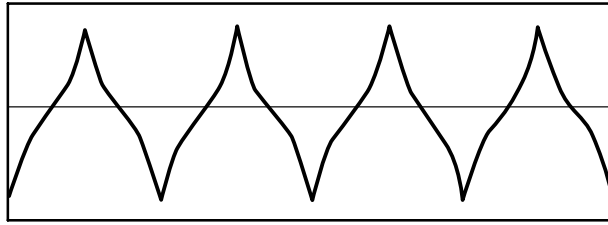


Figure 2. Pin Configuration

Table 2. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	REFOUT	O	Buffered output of the input frequency.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	XIN/CLKIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock
4	$V_{DD}$	P	Power supply for the entire chip (3.3 V).
5	ModOUT	O	Spread spectrum clock output.
6	$V_{SS}$	P	Ground connection.

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**Figure 3. Modulation Profile**

**Table 3. MAXIMUM RATINGS**

Symbol	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to Ground	0.5 to + 7.0	V
$T_{STG}$	Storage Temperature	-65 to +125	°C
$T_A$	Operating Temperature	0 to 70	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. DC ELECTRICAL CHARACTERISTICS** (Test Conditions: All parameters are measured at room temperature 25°C)

Symbol	Description	Min	Typ	Max	Unit
$V_{IL}$	Input LOW Voltage	GND - 0.3		0.8	V
$V_{IH}$	Input HIGH Voltage	2.0		$V_{DD} + 0.3$	V
$I_{IL}$	Input LOW Current			-35	μA
$I_{IH}$	Input HIGH Current			35	μA
$I_{XOL}$	XOUT Output LOW Current (@ 4.0 V, $V_{DD} = 3.3$ V)		3		mA
$I_{XOH}$	XOUT Output HIGH Current (@ 2.5 V, $V_{DD} = 3.3$ V)		3		mA
$V_{OL}$	Output LOW Voltage ( $V_{DD} = 3.3$ V, $I_{OL} = 20$ mA)			0.4	V
$V_{OH}$	Output HIGH Voltage ( $V_{DD} = 3.3$ V, $I_{OH} = 20$ mA)	2.5			V
$I_{DD}$	Static Supply Current (Note 1)			1.5	mA
$I_{CC}$	Dynamic Supply Current (3.3 V, 30 MHz, and 15 pF loading)			6	mA
$V_{DD}$	Operating Voltage	3.0	3.3	3.6	V
$t_{ON}$	Powerup Time (first locked cycle after powerup) (Note 2)			10	mS
$Z_{OUT}$	Clock Output Impedance		50		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. XIN/CLKIN pin is pulled low.
2.  $V_{DD}$  and XIN/CLKIN input are stable.

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**Table 5. AC ELECTRICAL CHARACTERISTICS**

Symbol	Description	Min	Typ	Max	Unit
CLKIN	Input Frequency	15		30	MHz
ModOUT	Output Frequency	15		30	MHz
REFOUT	Output Frequency	15		30	MHz
t <sub>LH</sub> (Note 3)	Output Rise Time (measured at 0.8 V to 2.0 V)	0.5	0.7	1.1	ns
t <sub>HL</sub> (Note 3)	Output Fall Time (measured at 2.0 V to 0.8 V)	0.5	0.7	1.0	ns
t <sub>JC</sub>	Jitter (Cycle-to-Cycle)			360	ps
t <sub>D</sub>	Output Duty Cycle	45	50	55	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. t<sub>LH</sub> and t<sub>HL</sub> are measured at capacitive load of 15 pF.

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## ORDERING INFORMATION

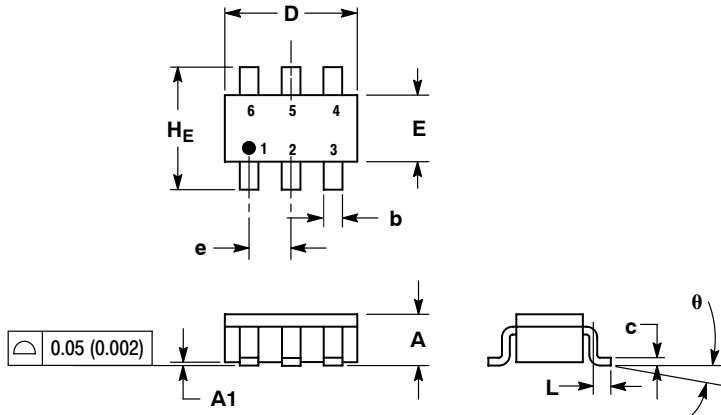
Device	Marking	Temperature Range	Package	Shipping†	Availability
NB2872ASNR2	E0A	0°C – 70°C	TSOP-6 (TSOT-23-6)	2500 Tape & Reel	<i>Now</i>
NB2872ASNR2G	E0A	0°C – 70°C	TSOP-6 (TSOT-23-6) (Pb-Free)	2500 Tape & Reel	<i>Contact Sales Representative</i>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

### TSOP-6 CASE 318G-02 ISSUE S

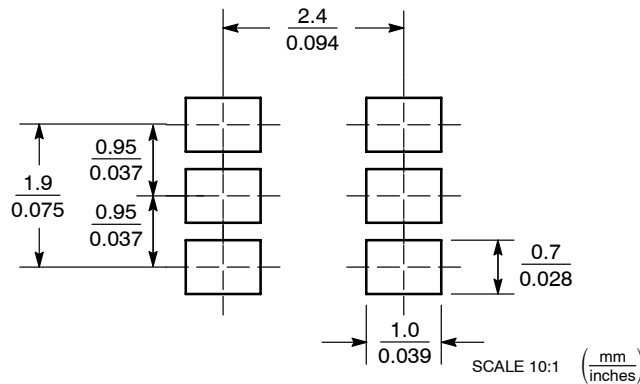


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, Dated 11-11-2003.

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